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(54) A method of fabricating a semiconductor device

(57) The present invention is related to Integrated Circuit (IC) processing and fabrication. A device and a method are provided for etching an opening in an insulating layer while depositing a barrier layer on the sidewalls of the opening without essentially depositing a barrier layer on the bottom of the opening.

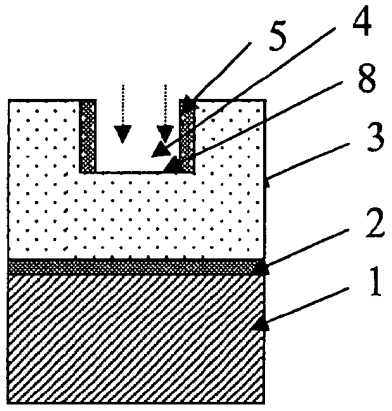

FIG. 2

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Description

Field of the Invention

[0001] The present invention is related to Integrated circuit (IC) processing and fabrication. A device and a method are provided for etching an opening in an insulating layer while depositing a barrier layer on the sidewalls of the opening without essentially depositing a barrier layer on the bottom of the opening.

Background of the Invention

[0002] Over the years, the demand for higher speed integrated circuits has been addressed through shrinkage of the device dimensions and increase of the packing density of the devices in integrated circuits or on carrier packages. By decreasing the layout rules of the devices, one can obtain transistors with higher intrinsic switching speed. In addition, putting the devices closer to each other reduces the communication time between transistor devices. Both approaches allow building circuits with increased overall performance, i.e., higher switching speed combined with higher functional circuits. Additionally, the integrated circuit area has increased, leading to circuits with even higher functionality as more devices can be integrated in a given area.

[0003] The structures connecting these devices can comprise multiple metal levels which are, depending upon the aimed interconnect pattern, either separated one from another by means of interlevel electrically insulating layers or connected one to the other by means of a conductive connection through these insulating layers. These insulating layers also take part in the separation of interconnect structures defined on the same metal level. Besides the downscaling of the dimensions of these interconnecting structures, additional measures are required to be able to meet the stringent speed specifications.

[0004] For future technologies the increasing impact of the back end processing in the fabrication of integrated circuits is recognized. A major change in back end processing is necessitated by the ever-decreasing feature size of the devices of integrated circuits that has indicated RC delay-time of the interconnect structures to be the limiting speed factor of the next generation of integrated circuits. To address this problem, two major routes are being explored: introduction of metals with higher conductivity and introduction of dielectric materials with lower dielectric constants.

[0005] The introduction of these materials has changed the outlook of the back end processing schemes where dry etch processes, cleaning recipes, and barrier requirements all need to be adapted

[0006] Although aluminum alloys and oxides are still widely used in interconnect technology, copper and new low-k dielectrics, e.g., polymers, are rapidly being implemented in microelectronics as they are now accepted as the future materials of choice. Copper offers a lower resistance and, depending on many processing parameters, this low resistivity can be combined with a better resistance to electromigration. The introduction of copper requires the introduction of damascene processing, which is an important change with respect to classical processing that uses patterning of the conductive elements. In damascene processing, trenches are formed in the insulating layers. After the patterning of the trenches, metal layers are deposited in the trenches and on top of the insulation layers. Finally, the metal layer is polished down to the top of the insulating layers, leaving only the via and trenches filled with metal.

[0007] The use of copper in interconnect structures has some commonly known disadvantages. Copper can diffuse very fast in the surrounding insulating layers, such as the low-k materials, which negatively affects the reliability and the signal delay. Several solutions have been proposed to solve this problem. The currently used techniques inhibit the migration of copper ions in the surrounding layers by depositing, in a non-selective way, diffusion barrier layers, e.g., refractory metals such as tantalum nitride (TaN), titanium nitride (TiN) in between the copper and the insulating layers. The horizontal, i. e. the bottom, as well as the vertical sidewalls of an opening in these insulating layers, e.g. a via or contact hole, are therefore covered with a barrier material. In case of Chemically Vapor Deposition (CVD) techniques, the barrier is conformal deposited. In case of Physical Vapor Deposition (PVD) techniques, the coverage of the vertical sidewalls of an opening and the bottom of this opening is less, compared to the coverage of the top of the opening. However, the ratio between side wall and horizontal coverage can be tuned to a certain extent by modifying the process parameters, such as deposition power and the bias of deposition.

[0008] Several problems are related to the above-mentioned process. Since a barrier layer is always deposited on both the vertical side walls and the bottom surface of an opening in the insulating layer, the presence of a barrier layer on the bottom of the opening causes several inconveniences. In order to ensure the conductivity of the metal lines, the barrier on the bottom of the opening must be made of an electrically conductive material. The adhesion between the barrier layer and the underlying conductive layer is not always good, thereby influencing the current flow between the different conductive levels. When the opening is afterwards filled with a metal in order to connect the metal layer underneath the insulating layer, the barrier layer between both metal layers has a detrimental effect on the electromigration behavior of the structure.

[0009] In addition, the exposure of the copper layers in the classical scheme to the dielectric etch plasma leads to the formation of residues on top of the copper. At the same time, copper sputtering, even though in very small amounts, and re-deposition onto the unprotected low-k sidewalls can not be avoided. Therefore, one has

to make use of after-etch cleaning methods to remove the copper from the side walls of the opening etched in the insulating low-k material in order to prevent copper diffusion into the low-k material. After etching of the barrier, further cleaning methods are needed to clean up the residues on top of the copper in order to obtain a good via resistance. The different cleaning methods that are used must be compatible with the presence of the low-k material and must avoid sputtering of copper onto the sidewalls of the opening.

[0010] In the damascene metallization scheme, the first step is a pre-clean of the copper surface, which can be an in-situ pre-clean. This step includes the high risk of having re-deposition of copper on the low-k sidewall, which may lead to its subsequent diffusion into the low-k material during the following barrier sputter process at higher temperature. In addition, it is clear that the pre-clean process step may also change the low k material properties leading to, e.g., an increased k value after the full process integration. The formation of TaN barrier layers with PVD techniques is difficult for high aspect ratio features, due to the intrinsic limited step coverage of such a process. Bad quality TaN barriers or layers which are too thin may lead to local breakdown of the copper barrier film and thus create a diffusion path for the copper.

[0011] The CMP process step makes use of two different slurries for, respectively, the CMP removal of copper and of the TaN. This makes the CMP process very difficult, very complex and very time- and slurry-consuming, resulting in a high cost of ownership with medium process quality only.

[0012] When an opening is formed in a porous insulating material, the pores of the insulating material at the sidewall of the opening are intersected, resulting in a rough sidewall. Subsequently, the barrier layer is deposited by, e.g., PVD on the sidewalls of the opening, resulting in a barrier layer with the same profile as the rough sidewall of the opening. This has a detrimental effect on the final device performance.

[0013] US-A-5818071 discloses interconnect structures incorporating a silicon carbide layer as a diffusion barrier layer, more specifically a layer between a dielectric and a highly conductive metal layer with a resistivity less than about 2.5 microhm-centimeters. US 5818071 does not disclose how to pattern or to remove the silicon carbide layer selectively to expose the underlying layer, more particularly a metal layer.

[0014] US-A-5904565 discloses a method for selectively forming barrier layers in a via or damascene structure after patterning these vias and damascene structures.

[0015] US-A-5176790 discloses an improved process for forming a via in an integrated circuit by etching through an insulating layer while inhibiting the sputtering of the underlying metal. Said process is performed by, e.g., using in the gaseous etchant one or more 3-6 carbon atom fluorinated hydrocarbons having the chemical formula $C_xH_yF_z$.

Summary of the Invention

[0016] The present invention is related to a method for etching an opening in an insulating layer while depositing a barrier layer on the sidewalls of said opening without essentially depositing a barrier layer on the bottom of said opening is therefore desirable.

[0017] In a first aspect of this invention, a method is disclosed for forming at least one opening in an insulating layer on a substrate while depositing a barrier layer on the sidewalls of said opening without essentially depositing said barrier layer on the bottom of said opening, comprising the steps of:

- subjecting said substrate to a plasma, said plasma being generated in a gaseous mixture comprising at least three components:
- a first component for depositing said metal barrier layer on at least the sidewalls of said opening,
- a second component for forming an opening in said insulating layer, and
- a third component for removing said barrier layer being formed on the bottom of said opening;
- etching said insulating layer with said plasma; and
- depositing said barrier layer on said sidewalls of said opening with said plasma.

[0018] The steps of etching and depositing are performed by controlling said plasma in a manner that while creating an opening in an insulating layer, a barrier layer is formed on the sidewalls of said opening without essentially forming a barrier layer on the bottom on said opening.

[0019] In an embodiment of this first aspect, a method as recited in the first aspect of this invention is disclosed wherein said first component comprises at least one of the group consisting of 1-methyl silane, 2-methyl silane, 3-methyl silane, 4-methyl-silane, a mixture of SiH_4 and N_2, a mixture of WF_6 and N_2, and combinations thereof.

[0020] In a further embodiment of this first aspect, a method as recited in the first aspect of this invention is disclosed wherein said second component comprises at least one of the group consisting of N_xO_y, $C_xF_yH_zO_u$, N_2/O_2, N_2/H_2, O_2, O_3, NH_3, CO, CO_2, CH_4, and combinations thereof.

[0021] In a further embodiment of this first aspect, a method as recited in the first aspect of this invention is disclosed wherein said third component comprises at least a chemical compound that form halogen ions or radicals in said etching plasma.

[0022] In a further embodiment of this first aspect, a method as recited in the first aspect of this invention is disclosed wherein said third component is at least one of the group consisting of NF_3, SF_6, F_2, ClF_3, and $C_xF_yH_z$.

[0023] In a further embodiment of this first aspect, a

method as recited in the first aspect of this invention is disclosed wherein said gaseous mixture further comprises an inert gas.

[0024] In a further embodiment of this first aspect, a method as recited in the first aspect of this invention is disclosed wherein said plasma is a continuous plasma.

[0025] In a further embodiment of this first aspect, a method as recited in the first aspect of this invention is disclosed wherein said plasma is a pulsed plasma.

[0026] In a further embodiment of this first aspect, a method as recited in the first aspect of this invention is disclosed wherein said barrier layer is a metal diffusion barrier layer. Preferably, said barrier layer is a copper diffusion barrier layer. Said barrier layer can be selected from the group consisting of Ti, TiN, Ta, TaN, $Ta_xSi_yN_z$, W_xN_y, $W_xC_yN_z$, SiC, SiOC, hydrogenated SiC, hydrogenated SiOC, and combinations thereof.

[0027] In a further embodiment of this first aspect, a method as recited in the first aspect of this invention is disclosed wherein said insulating layer comprises at least a porous material. Said insulating layer can be an organic containing insulating layer or an inorganic containing insulating layer.

[0028] In a further embodiment of this first aspect, a method as recited in the first aspect of this invention is disclosed wherein said opening is a via hole, said via hole extending through said insulating layer to an underlying conductive layer or an underlying barrier layer.

[0029] In a further embodiment of this first aspect, method as recited in the first aspect of this invention is disclosed wherein said method further comprises, prior to the step of subjecting said substrate, the steps of:

- covering said insulating layer with a bilayer, said bilayer comprising a resist hard mask layer being formed on the insulating layer and a resist layer being formed on the hard mask layer
- patterning said bilayer.

[0030] In a second aspect of this invention, a device is disclosed comprising an insulating layer on a substrate, said insulating layer having an opening, wherein sidewalls of said opening are covered with a barrier layer and a bottom of said opening is essentially not covered with said barrier layer, characterized in that said device is obtainable by a method comprising the steps of:

subjecting said substrate to a plasma, wherein said plasma is generated in a gaseous mixture comprising at least three components, said components comprising: a first component for depositing said metal barrier layer on at least the sidewalls of said opening, a second component for forming an opening in said insulating layer, and a third component for removing said barrier layer formed on the bottom of said opening;
etching said insulating layer with said plasma; and
depositing said barrier layer on said sidewalls of said opening with said plasma.

[0031] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed wherein said first component is selected from the group consisting of 1-methyl silane, 2-methyl silane, 3-methyl silane, 4-methyl-silane, a mixture of SiH_4 and N_2, and combinations thereof.

[0032] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed wherein said second component is selected from the group consisting of N_xO_y, $C_xF_yH_xO_u$, N_2/O_2 mixtures, N_2/H_2 mixtures, O_2, O_3, and combinations thereof.

[0033] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed wherein said third component comprises a chemical compound that forms a halogen ion or a radical in said plasma.

[0034] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed wherein said third component is selected from the group consisting of NF_3, SF_6, F_2, ClF_3, and mixtures thereof.

[0035] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed wherein said gaseous mixture further comprises an inert gas.

[0036] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed, wherein said plasma is a continuous plasma.

[0037] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed, wherein said plasma etching is a pulsed plasma.

[0038] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed wherein said barrier layer is a metal diffusion barrier layer.

[0039] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed, wherein said barrier layer comprises silicon carbide.

[0040] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed, wherein said insulating layer comprises a porous material.

[0041] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed wherein said insulating is an organic containing insulating layer.

[0042] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed, wherein said insulating layer is an inorganic containing insulating layer.

[0043] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is

disclosed wherein said opening is a via hole, said via hole extending through said insulating layer to an underlying conductive layer or an underlying barrier layer.

[0044] In an embodiment of this second aspect, a device as recited in the second aspect of the invention is disclosed the method for producing the device further comprising the steps of:

- covering said insulating layer with a bilayer, said bilayer comprising a resist hard mask layer formed on the insulating layer and a resist layer formed on the hard mask layer; and
- patterning said bilayer.

Brief Description of the Drawings

[0045] Figures 1 illustrate the prior method for forming an opening in an insulating layer and depositing a barrier layer on the sidewalls of the opening according to the prior art.

[0046] Figures 2 illustrate a method for forming an opening in an insulating layer while depositing a barrier layer on the side walls of the opening without essentially depositing a barrier layer on the bottom of the opening. The dashed arrows illustrate the anisotropic aspect of the plasma etching

Detailed Description of the Preferred Embodiment

[0047] The following description and examples illustrate preferred embodiments of the present invention in detail. Those of skill in the art will recognize that there are numerous variations and modifications of this invention that are encompassed by its scope. Accordingly, the description of preferred embodiments should not be deemed to limit the scope of the present invention.

[0048] In a first aspect of this invention, a method is disclosed for forming at least one opening in an insulating layer on a substrate while depositing a barrier layer on the sidewalls of said opening without essentially depositing said barrier layer on the bottom of said opening, the method comprising the steps of:

- subjecting said substrate to a plasma, said plasma being generated in a mixture comprising at least three components including:
- a first component for depositing said metal barrier layer on at least the sidewalls of said opening,
- a second component for forming said opening in said insulating layer, and
- a third component for removing said barrier layer being formed on the bottom of said opening;
- etching said insulating layer with said plasma; and
- depositing said barrier layer on said sidewalls of said opening with said plasma.

[0049] As referred to herein, the steps as disclosed in the first aspect of the invention are also called plasma etching or plasma etch process, thus including at least said subjecting step, etching step, and depositing step.

[0050] The steps of etching and depositing are performed by controlling said plasma in a manner that, while creating an opening in an insulating layer, a barrier layer is formed on the sidewalls of said opening without essentially forming a barrier layer on the bottom of said opening. The term "essentially" as used in this context means that the barrier layer on the bottom of the opening can be formed but is substantially removed by the plasma.

[0051] The term "barrier layer" should be understood as any layer being present on at least a part of the sidewalls of the opening. If the opening is filled with a material, the barrier layer should be understood to be a layer between the insulating layer and the material filling the opening. The barrier layer should essentially prevent the diffusion of the material filling the opening into the insulating layer.

[0052] The term "layer" should be understood to include any layer having a thickness of at least one molecule. Examples of a layer include, but are not limited to, a monolayer, a stack of monolayers, a film with a thickness less than than 50 nm, or a film with a thickness greater than 50 nm.

[0053] The method as described herein is performed in such a way as to obtain the formation of a barrier layer on at least a part of at least one of the side walls of the opening while etching an opening in the insulating layer. Preferably, the plasma is controlled in such a way that the barrier layer is formed as a permanent, adhesive layer on the sidewalls of the opening in the insulating material. This means that specific conditions of the plasma, such as the ion energy and bias, the temperature, and the pressure and the composition of the etching gas should be selected. Thus, the barrier layer on the side walls of the opening is essentially not etched during the process. Preferably, the composition of the gaseous mixture and the conditions are chosen so as to obtain removal of the barrier material that builds up at the bottom of the opening. To create an opening in the insulating layer, a plasma is used. Etching using a plasma typically results in anisotropic etching. To obtain plasma etching, the spontaneous etching is preferably negligible while the etch reaction is effectively stimulated by the ion bombardment. In other words, the lateral etch should be negligibly small compared to the vertical etch rate. Furthermore, the plasma should be controlled such that an opening is created in such a manner that while creating an opening, a barrier layer is formed on said sidewalls of said opening without essentially forming a barrier layer on said bottom of said opening. For the purpose of this invention, plasma etching is understood as plasma-assisted etching, reactive ion etching (RIE), or reactive ion beam etching (RIBE).

[0054] The gaseous etching mixture for plasma etching comprises at least three components:

a first component for depositing said barrier layer on at least the sidewalls of said opening, a second component for forming an opening in said insulating layer, and a third component for removing said barrier layer being formed on the bottom of said opening. Said first, second, and third component can be different chemical species. Said gaseous mixture can also comprise one or two components. If the gaseous component comprises one component, this component is for depositing said barrier layer on at least the sidewalls of said opening, for forming an opening in said insulating layer, and for removing said barrier layer being formed on the bottom of said opening. This means that the chemical composition and the corresponding physical behavior in a plasma should be pre-selected. If the gaseous mixture comprises at least two components, the first component should be defined as being selected (i) for depositing said barrier layer on at least the sidewalls of said opening and for forming an opening in said insulating layer, or (ii) for depositing said barrier layer on at least the sidewalls of said opening and for removing said barrier layer being formed on the bottom of said opening, or (iii) for forming an opening in said insulating layer and for removing said barrier layer being formed on the bottom of said opening. The second component is (i) for depositing said barrier layer on at least the sidewalls of said opening, or (ii) for forming an opening in said insulating layer, or (iii) for removing said barrier layer being formed on the bottom of said opening.

[0055] Various combinations of the first and the second component are possible.

[0056] Said substrate can be a partly processed or pristine wafer or slice of semi-conductive material, like Si, GaAs, Ge, or an insulating material, e.g. a glass slice or a conductive material. Said substrate can comprise a patterned conductive layer. Particularly, when said substrate is a partly processed wafer or slice, at least a part of an active and/or passive device can already be formed and/or at least a part of the structures interconnecting these devices can be formed.

[0057] Said insulating layer can be an organic-containing insulating layer or an inorganic insulating layer.

[0058] The invention as described in the first aspect of this invention is particularly relevant for semiconductor processing.

[0059] In a first aspect of this invention, a method is disclosed for forming at least one opening in an insulating layer on a substrate while depositing a barrier layer on the sidewalls of said opening without essentially depositing said barrier layer on the bottom of said opening, the method comprising the steps of:

subjecting said substrate to a plasma, said plasma being generated in a mixture comprising at least three components:

- a first component for depositing said barrier layer on at least the sidewalls of said opening,
- a second component for forming an opening in said insulating layer,
- a third component for removing said barrier layer being formed on the bottom of said opening;
- etching said insulating layer with said plasma; and
- depositing said barrier layer on said sidewalls of said opening with said plasma.

[0060] Said method can further comprise the step of filling said opening, the sidewalls of which are covered with a barrier layer, with a conductive material.

[0061] Said substrate can be a substrate used in semiconducting processing including, but not limited to, e. g., silicon substrates and germanium substrates. Said substrate can be a wafer, a structure in the process of IC fabrication, any layer on a substrate in the process of IC fabrication, a semiconducting layer, or a semiconducting layer in the process of IC fabrication.

[0062] The term "fabrication" refers to the patterning of structures. More particularly, the substrates can be subjected to damascene processing, dual damascene processing, or front-end processing, where front-end processing means providing contacting on the source, drain, or gate regions.

[0063] The term "opening" should be understood to include a via hole, trench, groove, or contact hole made in a substrate used in semiconductor manufacturing. If the opening is a via hole, the opening extends through said insulating layer to an underlying conductive layer or an underlying barrier layer. If the opening is a contact hole, said opening extends through said insulating layer to contact the underlying source, drain, or gate regions.

[0064] The term "insulating layer" refers to a layer or a stack of layers made of non-conductive material used to electrically isolate layers made of conductive material from each other. Said insulating layer may include silicon oxide, silicon nitride, and silicon oxynitride. Said insulating layer can also comprise silicon oxycarbide, with varying concentrations of oxygen, carbon and silicon, as well as hydrogenated silicon oxycarbide. Said insulating layer can also be an organic-containing material, including, but not limited to, organic containing materials containing benzyl groups, saturated carbon-carbon bounds, and the like. Said insulating layer can be made of porous material.

[0065] The barrier layer can be a layer or a stack of layers preventing the diffusion of conductive material (which fills the opening) into the insulating layer. The nature of the barrier layer is determined by the conductive material filling the opening. When the metal is copper, the barrier layer may include, but is not limited to, Ti, TiN, Ta, TaN, $Ta_xSi_yN_z$, W_xN_y, $W_xC_yN_z$, SiC, SiOC, hydrogenated SiC, hydrogenated SiOC, and combinations thereof. The thickness of the deposited barrier layer can be lower than 50 nm, lower than 20 nm, and preferably

lower than 10 nm. In the most preferred embodiment, the thickness of the barrier layer is between 1 and 5 nm. Said barrier layer is a permanent barrier layer; this means that the barrier layer remains essentially on the sidewalls of the opening after filling the opening. Said barrier layer should have a good adhesion to the sidewalls of the opening.

[0066] In the first aspect of a preferred embodiment, said mixture comprises at least three components. Said mixture can be a gaseous mixture. The term "components" should be understood to include the chemical molecules present in the reaction chamber and exposed to the plasma. By bringing at least those three components into the plasma, an opening is formed in the insulating layer. Further, a barrier layer is formed on the sidewalls of the opening.

[0067] A first component contains the chemistries accounting for the in-situ deposition of the barrier layer. For a SiC barrier layer, examples of the first component include, but are not limited to, 1-methyl silane (1MS), 2-methyl silane (2MS), 3-methyl silane (3MS), and 4-methyl-silane (4MS). For a W_xN_y barrier layer, the first component may include, but is not limited to, a mixture of WF_6 and N_2. For a Si_3N_4 barrier layer, the first component can be a mixture of SiH_4 and N_2.

[0068] A second component contains the chemistries accounting for the anisotropic etching of the insulating dielectric, thereby creating the opening. Examples of the third component are N_xO_y, $C_xF_yH_zO_u$, N_2/O_2, N_2/H_2, O_2, O_3, NH_3, CO, CO_2, CH_4, and combinations thereof.

[0069] A third component contains the chemistries accounting for the anisotropic etching of this barrier layer according to another embodiment of the invention. Said second component is able to form ions or radicals in a plasma and is able to react with the barrier layer on the bottom of said opening, such that volatile reaction products are formed. Examples of the second component are fluorine containing chemistries, e.g., NF_3, SF_6, F_2, ClF_3, and chlorine containing chemistries, with or with additives such as oxygen.

[0070] These etching plasmas can further comprise inert gasses such as helium and argon.

[0071] Various combinations of the above mentioned first component, second component, and third component are possible.

[0072] Said gaseous mixture can also comprise one or two components. If the gaseous component comprises one component, this component is for depositing said barrier layer on at least the sidewalls of said opening, for forming an opening in said insulating layer and for removing said barrier layer being formed on the bottom of said opening. If the gaseous mixture comprises at least two components, the first component should be defined as being selected (i) for depositing said barrier layer on at least the sidewalls of said opening and for forming an opening in said insulating layer, or (ii) for depositing said barrier layer on at least the sidewalls of said opening and for removing said barrier layer being formed on the bottom of said opening, or (iii) for forming an opening in said insulating layer and for removing said barrier layer being formed on the bottom of said opening. The second component is (i) for depositing said barrier layer on at least the sidewalls of said opening, or (ii) for forming an opening in said insulating layer or (iii) for removing said barrier layer being formed on the bottom of said opening. Various combination of the first and the second component are possible.

[0073] By subjecting said substrate to a plasma, etching of the insulating layer with said plasma and deposition of the barrier layer on said sidewalls of said opening with said plasma occurs. The plasma is selected so as to obtain an opening in the insulating layer and so as to obtain a deposition of the barrier layer on the sidewalls of the opening. This means that the etching gases, the temperature, the pressure, the ion energy and bias of the etching gases are pre-selected. Furthermore, the electron density of the plasma is selected by adjusting the power applied to the plasma, the frequency of the power, and the nature of the walls of the reactor and the inert gases. The gaseous etching mixture can comprise three components. The components are preferably volatile and contain the chemical atoms necessary for the formation of the barrier layer.

[0074] In plasma etching, the etched surface is subjected to an ion flux, oriented vertically to the wafer surface. In a plasma, radicals are also generated, but the radicals have a random distribution. This ion flux is present in a plasma that aims to obtain a high degree of anisotropy. The origin of the vertically oriented ion flux is found in the existence of the sheath potential between the bulk of the plasma and the wafer surface, whereas the bulk of the plasma is at a more positive potential than the wafer surface. In the bulk of the plasma, ions move in randomly distributed directions. Whenever they approach the sheath, however, the potential difference induces the ions to collide onto the wafer surface orthogonal to the wafer surface, as implied by the electrical field. The purpose of anisotropic etching is to induce etch reactions to occur in the presence of this ion flux and prevent etching, or cause deposition, on the surfaces that are not subjected to this ion flux. While etching the insulating layer, the insulating material is removed such that an opening is created. The opening is formed by a physical process (ion flux) and a chemical reaction. The ion flux accounts also for the immediate removal of the barrier layer on the bottom of said opening. The ion flux essentially avoids the build-up of a barrier layer on the bottom of the opening. The vertical side walls of the etched openings are preferably not subjected to this ion flux, and hence, etching will not occur.

[0075] Said etching plasma can be a continuous plasma, meaning that the excitation power is continuously applied to the mixture. Said plasma can also be interrupted. Therefore, the power applied to the gaseous mixture is applied for a defined period, e.g., in the range of from 1 ms to 10 ms. The time between the pulses

(duty cycle) depends on the specific plasma conditions.

[0076] It is also possible to apply a continuous low power and to apply a pulsed plasma.

[0077] The process as described herein protects the insulating layer from the etching plasma and, equally important, copper sputtering onto the side walls of the insulating layers becomes less likely because the copper diffusion barrier is already deposited. Furthermore, the process as disclosed in this aspect of the invention has the advantage in that the cleaning after barrier etch is facilitated as the insulating material is protected and there is no need for removal of the copper from the side walls of the opening.

[0078] Said invention can, prior to the plasma etching step, further comprise the steps (i) covering said insulating layer with a bilayer, said bilayer comprising a resist hard mask layer being formed on the insulating layer and a resist layer being formed on the hard mask layer (ii) patterning said bilayer. After the plasma etching process as described in this invention, the opening can be cleaned and subsequently filled with a conductive material. Said conductive material may include, but is not limited to, a metal such as copper, aluminium, gold, tungsten, and combinations thereof.

[0079] Figures 2 illustrate a preferred embodiment of this invention. There is provided a process for the formation of a opening (4) in an insulating layer (3) while forming a copper barrier layer (5) on the sidewalls (7) of said opening (4) without essentially forming a barrier layer on the bottom (8) of said opening. Said opening is a via hole in an insulating layer. The insulating layer covers an underlying conductive layer (2). The trench extends to the conductive layer. The conductive layer is formed on a substrate (1) subject to back-end IC processing.

[0080] According to an embodiment of the invention, the copper-barrier layer comprises a silicon carbide layer. For the purpose of this invention, silicon carbide is understood to include a layer composed of at least Si and C, e.g., SiC, or of at least Si, C, and O, i.e., a silicon oxycarbide, e.g., SiOC, or at least Si, C, and H, e.g., an amorphous hydrogenated silicon carbide such as SiC: H. The substrates are introduced into a pressurized chamber of a plasma-etch tool, such as a reactive ion etch (RIE) plasma tool, and then processed. The temperature in said chamber is preferably 600 degrees C or below, even more preferably below 400 degrees C. This temperature can also be in the range of from 100 to 600 degrees C.

[0081] The process is performed using plasma etching with a gaseous mixture comprising at least three components.

[0082] A first component contains the chemistries accounting for the in-situ deposition of the barrier layer. For SiC, examples of the first component include, but are not limited to, 1-methyl silane (1MS), 2-methyl silane (2MS), 3-methyl silane (3MS), and 4-methyl-silane (4MS).

[0083] A second component contains the chemistries accounting for the anisotropic etching of this barrier layer according to another embodiment of the invention. Examples of the second component include halogen-containing chemistries, e.g., NF_3, SF_6, F_2, ClF_3, and chlorine containing chemistries, with or without additives.

[0084] A third component contains the chemistries accounting for the anisotropic etching of the insulating dielectric, thereby creating the opening. Examples of the third component include N_xO_y, $C_xF_yH_xO_u$, N_2/O_2, N_2/H_2, O_2, O_3, and equivalent chemistries.

[0085] The amount of each component is preferably at least 0.1 % of the total mixture.

[0086] Typical ratios of these mixtures include, but are not limited to, 25/50/25.

[0087] These etching plasmas can further comprise inert gasses such as helium and argon.

[0088] The optimized process conditions, such as temperature, ion energy and bias, pressure, and composition of the plasma depend on the barrier layer to be deposited and on the insulation layer to be simultaneously etched. The type of barrier layer depends on the kind of metal used in the metallization process, e.g., copper, aluminum, and the like.

[0089] Figures 1 illustrate the process as known in the prior art while figures 2 illustrate the process according to the present invention. Compared to the prior art, the method of the invention minimizes the sputtering of copper onto the side walls of the insulating layers, since the sidewalls are protected by the deposited barrier layer. The process as disclosed in this aspect of the invention has facilitates the cleaning after the formation of the opening and there is no need for removal of the copper from the side walls of the opening.

[0090] In another embodiment of the present invention, the method as disclosed is used for the formation of a Copper-barrier layer while etching a porous insulating material being is present on a substrate. The substrates that are to be etched can be silicon substrates subject to damascene processing. In a first step, said substrate is subjected to a plasma, said plasma being generated in a gaseous mixture comprising three components : a first component for depositing a SiC barrier layer, a second component for creating an opening in the porous SILK layer and a third component for removing the SIC barrier layer being formed on the bottom of said opening.

[0091] By subjecting said substrate to said plasma, an opening is created in the porous insulating layer, and a SiC barrier layer is formed on the sidewall of the opening. Since the insulating layer is made of a porous material the sidewalls are rough. By applying using the method as described in this application, the opening in the sidewalls is filled in the first part of the insulating layer, and a barrier layer is formed on the sidewalls. This results in smooth sidewalls. In the prior art, when the opening is formed and subsequently the barrier layer is

deposited by, e.g., PVD, the barrier layer has the same profile as the rough sidewall of the opening. This has a detrimental effect on the final device performance.

[0092] According to a preferred embodiment of the invention, the copper-barrier layer comprises a silicon carbide layer. This silicon carbide is understood to be a layer composed of at least Si and C, e.g., SiC, or of at least Si, C, and O, i.e., a silicon oxycarbide, e.g., SiOC, or at least Si, C, and H, such as, e.g., amorphous hydrogenated silicon carbide, SiC:H.

[0093] The substrate comprises a wafer in the process of back-end IC processing. The insulating material is a porous low k dielectric, commercially available as porous SiLK™ (Dow Chemical). The porous insulating layer™ is covered with a hardmask material, e.g. SiO2, SiC, a combination of SiO2 and SiC, or a spin-on hardmask, on top of which photoresist is spun. The substrates are introduced in a pressurized chamber of a plasma-etch tool, such as a reactive ion etch (RIE) plasma tool and then processed. The temperature in said chamber is in the range from 15 to 40 degrees C. RF power settings range from 200 to 2200 W for both electrodes. Operating pressure is typically between 50 and 250 mTorr. The process is performed using plasma etching with a gaseous mixture comprising at least three components.

[0094] A first component contains the chemistries accounting for the in-situ deposition of the barrier layer. For SiC, 3-methyl-silane (3MS) or 4-methyl-silane (4MS) will be used.

[0095] A second component contains the chemistries accounting for the anisotropic etching of this barrier layer. Fluorine-containing gases such as CF_4, CHF_3, CH_2F_2 or CHF_3 will be used. Inorganic hardmask-opening is also performed using these gases in combination with an inert gas such as Argon, and O_2 and/or CO.

[0096] A third component contains the chemistries accounting for the anisotropic etching of the insulating dielectric thereby creating the opening. Preferred chemistries for this third component are N_2/O_2, N_2/H_2 and O_2, possibly combined with CH4 or C_2H_4 for enhanced sidewall passivation and hardmask selectivity.

[0097] The first step in the processing sequence is the hardmask-opening. Secondly, the porous SiLK is etched while a SiC layer is deposited on the sidewalls. To propagate the etching, it is preferred to continuously remove the SiC at the bottom of the etched feature, until the SiC Cu diffusion barrier is reached. Finally, this barrier is etched anisotropically, so as not to remove the SiC on the sidewalls.

[0098] In another embodiment of this invention, a method is disclosed for forming at least one opening in an insulating layer on a substrate while depositing a barrier layer on the sidewalls of said opening, the method comprising the steps of:

- subjecting said substrate to a plasma, said plasma being generated in a mixture comprising at least two components:
- a first component for depositing said barrier layer on at least the sidewalls of said opening, and
- a second component for forming an opening in said insulating layer;
- etching said insulating layer with said plasma; and
- depositing said barrier layer on said sidewalls of said opening with said plasma.

[0099] Contrary to the embodiments described previously, in this embodiment it is not necessary to remove the barrier layer from the bottom of said opening. This is particularly relevant when the barrier layer is made of a conductive material.

[0100] The various aspects of this embodiment are similar to those of previously described preferred embodiments, with the exception that the gaseous mixture does not comprise a third component.

[0101] In a second aspect of this invention, a device is disclosed. Said device comprises an insulating layer on a substrate, said insulating layer having an opening, the sidewalls of said opening being covered with a barrier layer, wherein the bottom of said opening is essentially not covered with said barrier layer. Said device is obtainable by a method comprising the steps of:

- subjecting said substrate to a plasma, said plasma being generated in a gaseous mixture comprising at least three components:
- a first component for depositing said metal barrier layer on at least the sidewalls of said opening,
- a second component for forming an opening in said insulating layer, and
- a third component for removing said barrier layer being formed on the bottom of said opening;
- etching said insulating layer with said plasma; and
- depositing said barrier layer on said sidewalls of said opening with said plasma.

[0102] The scope of the method is determined by the disclosure of the first aspect of the invention.

[0103] In an embodiment of the second aspect of this invention, a device is disclosed, said device comprising a porous insulating layer on a substrate, said porous insulating layer having an opening, the sidewalls of said opening being covered with a barrier layer wherein the bottom of said opening is essentially not covered with said barrier layer. Said device is obtainable by a method comprising the steps of:

- subjecting said substrate to a plasma, said plasma being generated in a gaseous mixture comprising at least three components:
- a first component for depositing said metal barrier layer on at least the sidewalls of said opening,
- a second component for forming an opening in said insulating layer, and
- a third component for removing said barrier layer

being formed on the bottom of said opening;
- etching said insulating layer with said plasma; and
- depositing said barrier layer on said sidewalls of said opening with said plasma.

[0104] In the prior art, etching an opening in an insulating material would result in rough openings, since the pores of the insulating material are intersected by the plasma. When the barrier layer is subsequently deposited by a technique known in the prior art, e.g., PVD, the barrier layer has the same profile as the rough sidewall of the opening. This has a detrimental effect on the final device performance. By applying the method as described above, the opening in the sidewalls are filled in the first part of the insulating layer, and a barrier layer will be formed on the sidewalls. This results in smooth sidewalls.

[0105] The device as disclosed in an embodiment of the second aspect of this invention is characterized in that the pores that are intersected by the plasma during the formation of the opening are filled with material forming the barrier layer and that a barrier layer, preferably a thin layer, is formed on the sidewalls such that the sidewalls are essentially smooth.

[0106] The above description discloses several methods and materials of the present invention. This invention is susceptible to modifications in the methods and materials. Such modifications will become apparent to those skilled in the art from a consideration of this disclosure or practice of the invention disclosed herein. Consequently, it is not intended that this invention be limited to the specific embodiments disclosed herein, but that it cover all modifications and alternatives coming within the true scope and spirit of the invention as embodied in the attached claims. The disclosures of all references cited herein are hereby incorporated by reference in their entireties.

Claims

1. A method for forming at least one opening in an insulating layer on a substrate while depositing a barrier layer on sidewalls of said opening without essentially depositing said barrier layer on a bottom of said opening, the method comprising the steps of:

   - subjecting said substrate to a plasma, said plasma being generated in a gaseous mixture comprising at least three components, said components comprising a first component for depositing said barrier layer on at least the sidewalls of said opening, a second component for forming an opening in said insulating layer, and a third component for removing said barrier layer being formed on the bottom of said opening;
   - etching said insulating layer with said plasma; and
   - depositing said barrier layer on said sidewalls of said opening with said plasma.

2. A method as recited in claim 1, wherein said first component is selected from the group consisting of 1-methyl silane, 2-methyl silane, 3-methyl silane, 4-methyl-silane, a mixture of SiH4 and N_2, and combinations thereof.

3. A method as recited in claim 1 or 2 wherein said second component is selected from the group consisting of N_xO_y, $C_xF_yH_xO_u$, N_2/O_2 mixtures, N_2/H_2 mixtures, O_2, O_3, and combinations thereof.

4. A method as recited in anyone of the claims 1 to 3, wherein said third component comprises a chemical compound that forms a halogen ion or a radical in said plasma.

5. A method as recited in claim 4, wherein said third component is selected from the group consisting of NF_3, SF_6, F_2, ClF_3, and mixtures thereof.

6. A method as recited in anyone of the claims 1 to 5, wherein said gaseous mixture further comprises an inert gas.

7. A method as recited in anyone of the claims 1 to 6, wherein said plasma is a continuous plasma.

8. A method as recited in anyone of the claims 1 to 6, wherein said plasma is a pulsed plasma.

9. A method as recited in anyone of the claims 1 to 8, wherein said barrier layer is a metal diffusion barrier layer.

10. A method as recited in claim 9, wherein said barrier layer comprises at least silicon carbide.

11. A method as recited in anyone of the claims 1 to 10, wherein said insulating layer comprises a porous material.

12. A method as recited in anyone of the claims 1 to 11, wherein said insulating layer is an organic containing insulating layer.

13. A method as recited in anyone of the claims 1 to 11, wherein said insulating layer is an inorganic containing insulating layer.

14. A method as recited in anyone of the claims 1 to 13, wherein said opening is a via hole, said via hole extending through said insulating layer to an underlying conductive layer or to an underlying barrier lay-

er.

15. A method as recited in anyone of the claims 1 to 14, further comprising the steps of:

- covering said insulating layer with a bilayer, said bilayer comprising a resist hard mask layer formed on the insulating layer and a resist layer formed on the hard mask layer; and
- patterning said bilayer.

16. A device comprising an insulating layer on a substrate, said insulating layer having an opening, wherein sidewalls of said opening are covered with a barrier layer and a bottom of said opening is essentially not covered with said barrier layer, **characterized in that** said device is obtainable by a method comprising the steps of:

- subjecting said substrate to a plasma, wherein said plasma is generated in a gaseous mixture comprising at least three components; said components comprising: a first component for depositing said barrier layer on at least the sidewalls of said opening, a second component for forming an opening in said insulating layer, and a third component for removing said barrier layer formed on the bottom of said opening;
- etching said insulating layer with said plasma; and
- depositing said barrier layer on said sidewalls of said opening with said plasma.

17. A device as recited in claim 16, wherein said barrier layer is a metal diffusion barrier layer.

18. A device as recited in claim 17, wherein said barrier layer comprises silicon carbide.

19. A device as recited in anyone of the claims 16 to 18, wherein said insulating layer comprises a porous material.

20. A device as recited in anyone of the claims 16 to 19, wherein said insulating layer is an organic containing insulating layer.

21. A device as recited in anyone of the claims 16 to 20, wherein said insulating layer is an inorganic containing insulating layer.

22. A device as recited in anyone of the claims 16 to 21, wherein said opening is a via hole, said via hole extending through said insulating layer to an underlying conductive layer or an underlying barrier layer.

23. A gaseous mixture comprising at least three components in order to generate a plasma wherein is placed a device comprising an insulating layer on a substrate, **characterized in that** said components comprising; a first component for depositing said barrier layer on at least the sidewalls of said opening, a second component for forming an opening in said insulating layer, and a third component for removing said barrier layer formed on the bottom of said opening.

24. A mixture device as recited in claim 23, wherein said first component is selected from the group consisting of 1-methyl silane, 2-methyl silane, 3-methyl silane, 4-methyl-silane, a mixture of SiH_4 and N_2, and combinations thereof.

25. A mixture as recited in claim 23 or 24, wherein said second component is selected from the group consisting of N_xO_y, $C_xF_yH_xO_u$, N_2/O_2 mixtures, N_2/H_2 mixtures, O_2, O_3, and combinations thereof.

26. A mixture as recited in anyone of the claims 23 to 25, wherein said third component comprises a chemical compound that forms a halogen ion or a radical in said plasma.

27. A device as recited in claim 26, wherein said third component is selected from the group consisting of NF_3, SF_6, F_2, ClF_3, and mixtures thereof.

28. A device as recited in anyone of the claims 23 to 27, wherein said gaseous mixture further comprises an inert gas.

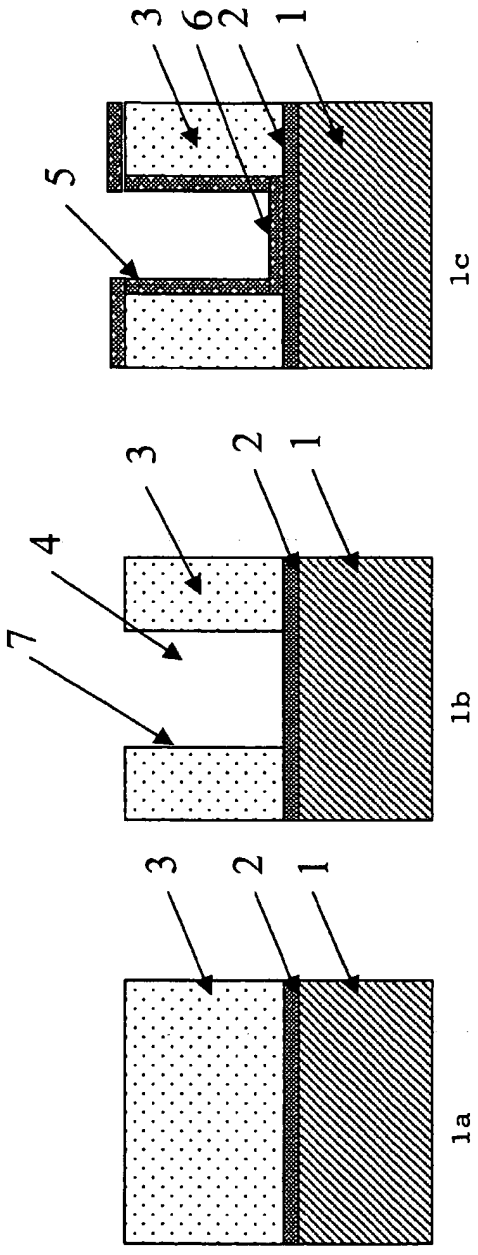

FIG. 1

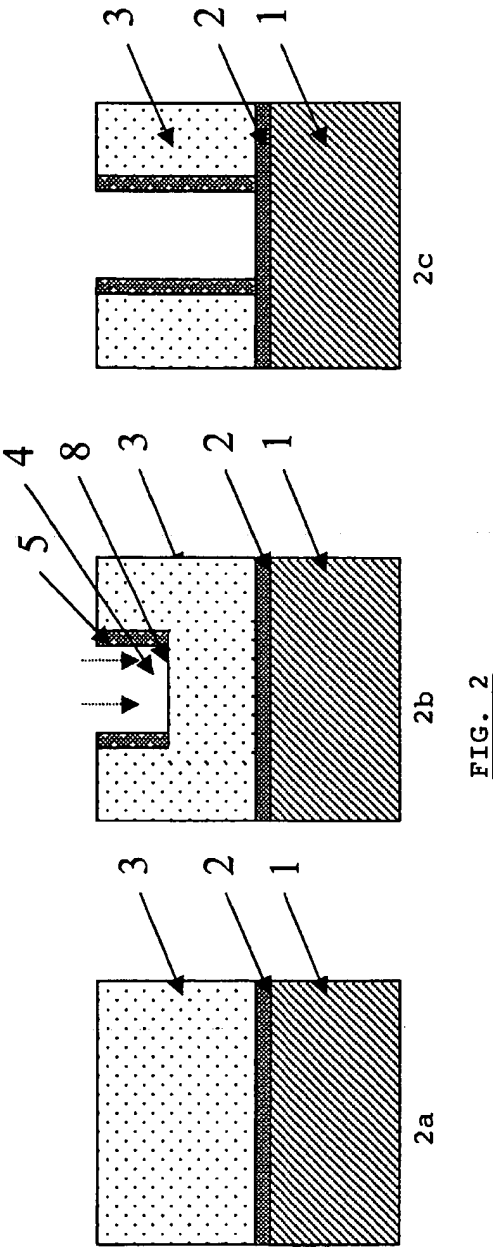

FIG. 2

PAT-NO: JP409063989A

DOCUMENT-IDENTIFIER: JP 09063989 A

TITLE: SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUBN-DATE: March 7, 1997

INVENTOR-INFORMATION:
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ASSIGNEE-INFORMATION:

NAME	COUNTRY
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APPL-NO: JP07233342

APPL-DATE: August 18, 1995

INT-CL (IPC): H01L021/28, H01L021/306 , H01L021/768

ABSTRACT:

PROBLEM TO BE SOLVED: To form a highly reliable contact on which no irregularity is generated on the side face of the contact even when a wet etching treatment is conducted for the purpose of mitigating the damage of etching when a contact hole is formed on a multilayer insulating film consisting of two or more kinds of insulating films.

SOLUTION: When a contact hole is perforated on the thin layer film consisting of a SiO<SB>2</SB> film 12, a SiN film 4 and a SiO<SB>2</SB> film 2, a side wall is formed on the side face of the contact hole using the

SiO<SB>1</SB>, which is the kind same as the bottom layer, after the aperture
has been formed to the middle part of the bottom layer of SiO<SB>2</SB> layer
by conducting an anisotropic dry etching, and then the contact surface is
exposed by wet etching SiO<SB>2</SB> using buffered hydrofluoric acid. At this
time, as no rugged part is formed on the side face of the contact hole, barrier
metal can be formed by a sputtering method without damaging the coverage of the
barrier metal. Subsequently, a metal plug and wiring metal are formed, and the
contact is completed.